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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,106	11/20/2003	Nai-Shung Chang	VIAP0108USA	1105

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EXAMINER	
NGUYEN, THAN VINH	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,106	CHANG ET AL.	
	Examiner	Art Unit	
	Than Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2006*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a response to the response, filed 3/28/06.

2. Claims 1-11 are pending.

Response to Arguments

3. Applicant's arguments filed 3/28/06 have been fully considered but they are not persuasive. Applicant argues that the prior art cited does not teach a single-channel memory controller. The Examiner disagrees. The claimed limitation is a memory controller that is named "a single-channel". No other details are given regarding what the controller does nor its composition. Thus, for examination purposes, the Examiner interprets this claimed limitation as a memory controller that is named "a signal-channel memory controller". Since Gupta also teaches a memory controller that is connected to memory slots and buses, Gupta meets the claimed invention. The Examiner maintains the previous prior art rejection to the claims.

Claim Rejections - 35 USC § 102

4. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Gupta et al (US 6,272,594).

As to claim 1:

5. Gupta teaches a memory-interleaving scheme. Gupta teaches a motherboard comprising: at least a first memory slot (slot 0-11; Fig. 2); at least a second memory slot (slot 12-23; Fig. 2); and a single-channel memory controller (memory controller 22; Fig. 2; 7/50-63) electrically

connected to the first memory slot and the second memory slot through a first bus (bus 0; Fig. 2) and a second bus (bus 1; Fig. 2; 7/65-8/5).

As to claim 2,6:

Gupta teaches each of the first and second buses is used for transferring memory data, memory addresses, and control signals (buses 0 and 1 carry data, address, and control signals to access DRAM; 2/45-67; 7/65-8/21).

As to claim 3,7:

6. Gupta teaches the single-channel memory controller comprises: a memory data input/output port for outputting a memory data to the first and second memory slots through the first and second buses (output of memory controller to buses to memory slots are all in memory bus; Fig. 2); a memory address output port for outputting a memory address to the first and second memory slots through the first and second buses; and a control signal output port for outputting a control signal to the first and second memory slots through the first and second buses (addresses and control signals go through bus 0 or 1; 2/45-67; 7/65-8/21).

As to claim 4,8:

7. Gupta teaches the single-channel memory controller is positioned inside a package, and the package comprises: at least two first external contacts connected to the first and second buses respectively for transferring memory data; at least two second external contacts connected to the first and second buses respectively for transferring memory addresses; at least two third external contacts connected to the first and second buses respectively for transferring control signals; and

a plurality of traces electrically connected to the first external contacts and a memory data input/output port of the single-channel memory controller, electrically connected to the second external contacts and a memory address output port of the single-channel memory controller, and electrically connected to the third external contacts and a control signal output port of the single-channel memory controller (memory controller 22 is a single package; Fig. 2, and has contacts/links to memory buses to carry data, address, and controller signals to memory slots; 7/65-8/21).

As to claim 5:

8. Gupta teaches at least a first dynamic random access memory (DRAM; 5/50-55; 6/48-55; 14/41); at least a second dynamic random access memory (DRAM; 5/50-55; 6/48-55; 14/41); and a single-channel memory controller (memory controller 22; Fig. 2; 7/50-63) connected to a first bus and a second bus respectively for controlling the first dynamic random access memory and the second dynamic random access memory (buses 0 and 1; Fig. 2; 7/65-8/5).

As to claim 9:

9. Gupta teaches a package comprising: a single-channel memory controller (memory controller 22; Fig. 2; 7/50-63); a plurality of first external contacts electrically connected to a memory data input/output port, a memory address output port, and a control signal output port of the single-channel memory controller, the first external contacts being used for connecting a first memory bus; and a plurality of second external contacts electrically connected to the memory data input/output port, the memory address output port, and the control signal output, the second external contacts being used for connecting a second memory bus (memory controller 22 is a

single package; Fig. 2, and has contacts/links to memory buses to carry data, address, and controller signals to memory slots; 7/65-8/21).

As to claim 10:

10. Gupta teaches the first memory bus (bus 0) is used for controlling a first memory slot (slots 0-11), and the second memory bus (bus 1) is used for controlling a second memory slot (slot 12-23).

As to claim 11:

11. Gupta teaches the first memory bus (bus 0) is used for controlling a first dynamic random access memory (DRAM 5/50-55; 6/48-55), and the second memory bus (bus 1) is used for controlling a second dynamic random access memory (DRAM 5/50-55; 6/48-55).

Conclusion

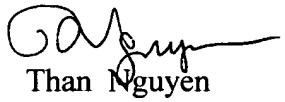
12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Than Nguyen can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Than Nguyen
Primary Examiner
Art Unit 2187